WHAT IS CLAIMED IS:

1. A microelectronic device, comprising:

a first semiconductor substrate bonded to a second semiconductor substrate, the first semiconductor substrate including an opening through which an epitaxially grown portion of the second semiconductor substrate extends;

a first semiconductor device coupled to the first semiconductor substrate; and

a second semiconductor device coupled to the epitaxially grown portion of the second semiconductor substrate.

2. The device of claim 1 wherein the first semiconductor device comprises a p-type transistor and the second semiconductor device comprises an n-type transistor.

3. The device of claim 1 wherein the first semiconductor device comprises an n-type transistor and the second semiconductor device comprises a p-type transistor.

4. The device of claim 1 wherein the first and second semiconductor substrates have different crystallographic orientations.

5. The device of claim 1 wherein the first semiconductor substrate has a (1,1,0) crystallographic orientation and the second semiconductor substrate has a (1,0,0) crystallographic orientation.

6. The device of claim 1 wherein the first semiconductor substrate has a (1,0,0) crystallographic orientation and the second semiconductor substrate has a (1,1,0) crystallographic orientation.

7. The device of claim 1 further comprising a dielectric film interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate.

8. The device of claim 1 further comprising a shallow trench isolation interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate, the shallow trench isolation spanning the thickness of the first semiconductor substrate and extending into the second semiconductor substrate.

9. The device of claim 1 further comprising an oxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the oxide layer.

10. The device of claim 1 further comprising a silicon dioxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the silicon dioxide layer.

11. The device of claim 1 further comprising an implanted oxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the implanted oxide layer.

12. The device of claim 1 wherein the first semiconductor substrate is a silicon-on-insulator substrate.

13. A method of manufacturing a microelectronic device, comprising:

coupling a first semiconductor substrate to a second semiconductor substrate;

patterning an opening in the first semiconductor substrate;

growing epitaxially an extension of the second semiconductor substrate through the opening;

forming a first semiconductor device on the first semiconductor substrate; and

forming a second semiconductor device on the extension of the second semiconductor substrate.

14. The method of claim 13 wherein the first semiconductor device comprises a p-type transistor and the second semiconductor device comprises an n-type transistor.

15. The method of claim 13 wherein the first semiconductor device comprises an n-type transistor and the second semiconductor device comprises a p-type transistor.

16. The method of claim 13 wherein the first and second semiconductor substrates have different crystallographic orientations.

17. The method of claim 13 wherein the first semiconductor substrate has a (1,1,0) crystallographic orientation and the second semiconductor substrate has a (1,0,0) crystallographic orientation.

18. The method of claim 13 wherein the first semiconductor substrate has a (1,0,0) crystallographic orientation and the second semiconductor substrate has a (1,1,0) crystallographic orientation.

19. The method of claim 13 further comprising forming a dielectric film on the first semiconductor substrate opposite the second semiconductor substrate and one at least a portion of a surface of the opening before epitaxially growing the extension of the second semiconductor substrate.

20. The method of claim 19 further comprising planarizing the first semiconductor substrate, the dielectric film, and the extension of the second semiconductor substrate to form a substantially planar surface collectively therefrom.

21. The method of claim 20 wherein planarizing includes substantially removing all of the dielectric film not located in the opening.

22. The method of claim 13 further comprising forming a shallow trench isolation separating the first semiconductor substrate and the extension of the second semiconductor substrate, the shallow trench isolation spanning the thickness of the first semiconductor substrate and extending into the second semiconductor substrate.

23. The method of claim 13 further comprising forming an oxide layer proximate an interface between the first semiconductor substrate and the second semiconductor substrate prior to forming the opening, the opening also extending through the oxide layer.

24. The method of claim 23 wherein forming the oxide layer includes implanting an oxide through at least a portion of the first semiconductor substrate, the opening also extending through the implanted oxide layer.

25. The method of claim 13 wherein coupling the first semiconductor substrate to the second semiconductor substrate includes bonding the first semiconductor substrate to the second semiconductor substrate.

26. The method of claim 25 wherein the first and second semiconductor substrates comprise first and second wafers, respectively, and wherein bonding comprises wafer bonding.

27. An integrated circuit device, comprising:

a first semiconductor substrate having a plurality of openings extending therethrough;

a second semiconductor substrate coupled to the first semiconductor substrate and including a plurality of epitaxially grown extensions each extending through a corresponding one of the plurality of openings;

a plurality of first semiconductor devices each coupled to the first semiconductor substrate; and

a plurality of second semiconductor devices each coupled to a corresponding one of the plurality of extensions.

28. The integrated circuit device of claim 27 wherein ones of the plurality of first semiconductor devices each comprise a p-type transistor and ones of the plurality of second semiconductor devices each comprise an n-type transistor.

29. The integrated circuit device of claim 27 wherein ones of the plurality of first semiconductor devices each comprise an n-type transistor and ones of the plurality of second semiconductor devices each comprise a p-type transistor.

30. The integrated circuit device of claim 27 wherein the first and second semiconductor substrates have different crystallographic orientations.

31. The integrated circuit device of claim 27 wherein the first semiconductor substrate has a (1,1,0) crystallographic orientation and the second semiconductor substrate has a (1,0,0) crystallographic orientation.

32. The integrated circuit device of claim 27 wherein the first semiconductor substrate has a (1,0,0) crystallographic orientation and the second semiconductor substrate has a (1,1,0) crystallographic orientation.

33. The integrated circuit device of claim 27 further comprising a plurality of dielectric films each interposing a sidewall of one of the plurality of openings and a corresponding one of the plurality of extensions of the second semiconductor substrate.

34. The integrated circuit device of claim 27 further comprising a plurality of shallow trench isolation structures each interposing a sidewall of one of the plurality of openings and a corresponding one of the plurality of extensions of the second semiconductor substrate, spanning the thickness of the first semiconductor substrate, and extending at least partially into the second semiconductor substrate.

35. The integrated circuit device of claim 27 further comprising an oxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the plurality of openings each also extending through the oxide layer.

36. The integrated circuit device of claim 35 wherein the oxide layer comprises silicon dioxide.

37. The integrated circuit device of claim 35 wherein the oxide layer comprises an implanted oxide layer.

38. The integrated circuit device of claim 27 wherein at least one of the first and second semiconductor substrates is a silicon-on-insulator substrate.